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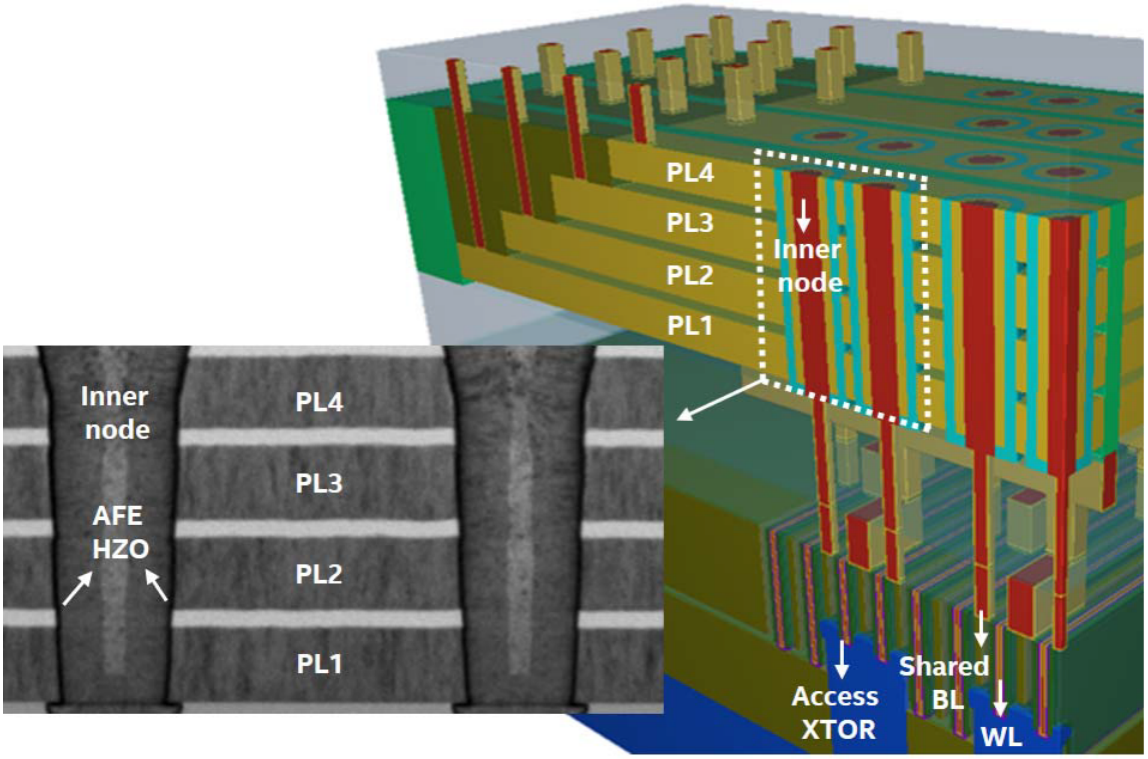
3D DRAM

Over the course of 2021 and early 2022 various DRAM participants have begun to discuss 3D DRAM, although few examples have been presented at technical conferences, and it appears that very few prototypes have been reduced to silicon.

Figure 7 illustrates a cross-section of a 3D DRAM approach actually prototyped by Intel and presented at the 2020 IEEE International Electron Devices meeting (IEDM).

Figure 7. Intel's Antiferroelectric DRAM



Source: Intel Corp. Used with Permission

This design harnesses 3D NAND manufacturing techniques, but replaces the floating gate that Intel used in its 3D NAND flash with a DRAM capacitor based on an antiferroelectric hafnium-oxide (HfO) dielectric. Antiferroelectrics are an application of standard ferroelectric materials. Ferroelectric materials, in addition to being useful as nonvolatile memory elements (discussed in detail later in this report), also have a dielectric constant about an order of magnitude larger than the dielectric materials currently used in production DRAM. The area of the DRAM's capacitor is inversely proportional to the dielectric constant, allowing Intel's 3D DRAM to have a capacitor that fits within the dimensions of this format of 3D bit cell. Today ferroelectric HfO is poorly understood and cannot therefore be used for mass production, but this technology is receiving significant attention, and many expect ferroelectric HfO to become production-worthy within only a few years.

Other approaches include:

- The simple flipping of existing structures with existing materials
- The use of the floating body effect which Unisantis has dubbed the “Dynamic Flash Memory” or DFM
- Vertical capacitors layered above vertical select transistors similar to the transistors in 3D NAND but with epitaxial channels rather than the polysilicon channels used in 3D NAND
- Capacitorless 2-transistor gain cells
- And even 3D NAND flash that trades off write speed for a very short retention time that must be refreshed like a standard DRAM.

All of these technologies promise to extend DRAM bit scaling by at least a few more generations to forestall any possible conversion of the DRAM market to an alternative technology like MRAM.

Should DRAM convert to a 3D approach, then it is reasonable to expect delays similar to those suffered by NAND flash when it transitioned from planar to 3D strings. This was a very costly transition, since the process changed from lithography-intensive to deposition/etch intensive, driving very significant retooling costs, and it was a very slow transition as altogether new technologies needed to be put into high-volume production. In the end, the transition occurred three years later than originally intended.

The transition to 3D NAND did succeed in preventing an anticipated switch from NAND flash to stacked ReRAM, though, and DRAM’s 3D transition is quite likely to have a similar outcome.